Amendments to the Specification

Please replace the paragraph beginning on page 22 line 1, with the following amended paragraph:

When the first input voltage 412 is lower than the reference input voltage 422, the first output voltage signal 418 is pulled high to turn on the MOS transistor 426 and to supply current from the high voltage source 423 to the cell plate voltage, VEQ 136. When the second input voltage 414 is higher than the reference input voltage 422, the second output voltage signal 420 is pulled high to turn on the MOS transistor 428 and the current is sunk from the cell plate voltage, VEQ 136, to the low voltage source 424. The voltage generator 400 doesn't supply or sink current for the cell plate voltage, VEQ 136, in a well-defined range. The range is given by

~~VCC-(VCC-Vref)*(R1+R1+R3)/R1 < VEQ < VCC-(VCC-Vref)*R1+R2+R3)/(R1+R2)~~

VCC-(VCC-Vref)*(R1+R1+R3)/R1 < VEQ < VCC-(VCC-Vref)*(R1+R2+R3)/(R1+R2)

where VCC is, for example, the high reference voltage 416; Vref is the reference input voltage 422; and R1 456, R2 458, and R3 460 are the resistors in the voltage dividing circuit 402.